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Picturephone® Silicon Target Signal Analysis

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Signal characteristics of the silicon diode array used as the image sensing element of the Picturephone® camera tube have been studied using a numerical computation. Analytical representation of the target is based on the numerical calculation of the depletion region geometry for an array diode unit-cell undergoing discharge. This analysis includes the effects of Si–SiO_2 fixed interface charge density, sea resistance, substrate resistivity, P^+ island geometry, and SiO_2–Si surface inversion phenomenon.

Computed depletion region geometries are used to calculate surface and bulk contributions to array dark current. It is shown that signal current limitations due to surface inversion can be avoided using lower values of sea resistance coupled with higher SiO_2–Si interface fixed charge density. For the resistive sea target structure, inversion effects are less pronounced for targets fabricated with P^+ islands larger than 10 μm diameter and sea sheet resistances less than 10^{14} ohms per square. This signal limiting effect can also be eliminated by using a conductive overlay structure.

Results of analyses of lag characteristics and electron beam limitations are also presented.

I. INTRODUCTION

The silicon target, used as the image sensing element in the *Picturephone*® camera tube,[1–4] is composed of a matrix of diffused diodes.

Signal characteristics of the target are the result of a complex interaction of the material and geometric parameters of the individual array diodes as well as the operating conditions of the target. We have analtyically investigated target signal characteristics by means of numerical computations, solving explicitly for depletion region geometry and capacitance and have determined signal characteristics as a function of Si–SiO_2 interface fixed charge density, sea resistance*, substrate resistivity, P^+ island geometry, SiO_2–Si surface inversion phenomenon, and electron beam acceptance characteristics.

Section II describes the diode array format and the basic relationship of signal current to array capacitance. The model of the reversed biased unit cell and the mathematic analysis are described in Sections II and III. Signal capabilities of a resistive sea diode array structure are discussed in Section IV and extended to include the effects of electron beam acceptance in Section V. An alternate geometric structure using conductive overlays is analyzed in Section VI. The relationship between the array dark current characteristic and target parameters is presented in Section VII. In the concluding section we present experimental verification of the model.

II. GENERAL TARGET OPERATION

The *Picturephone*® camera tube target is an array of 8×10^5 planar P^+N diodes fabricated on a thin N-type silicon membrane, (Fig. 1). The optical sensing mechanism of the target is the discharge

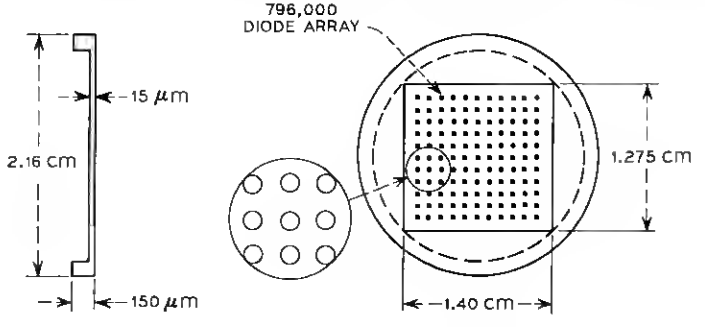

Fig. 1—Silicon camera tube target.

* We use the term "sea" to describe the resistive layer covering the array surface containing the P^+ diffused regions which we will refer to as P^+ islands.

of this array of diodes by light incident on the N^+ surface (side opposite the array). To review the details of the operation it is convenient to consider an individual array element, or unit cell, represented by a 15μm square section of the array containing a centrally located diode.

The back surface of the target is held at a potential V_T. The target face potential is periodically reduced to ground potential by the scanning electron beam (Fig. 2). For ideal beam acceptance, the target unit cell (consisting of the junction plus the oxide capacitance) is reverse biased by an amount V_T immediately after scanning. At this time, the junction depletion region and any existing silicon surface depletion region will be at their geometric maximum. During the time interval (corresponding to a frame time, τ_F), that the electron beam is scanning the remainder of the target, the diode cell is discharged by the photon generated holes which diffuse to the depletion region of the device.

The relationship between light-generated minority carriers available for discharge and the incident photon flux and the subsequent diffusion of these carriers to the diode depletion region has been discussed by others.[4] The individual diode steady state signal current can be related to the diode discharge by

$$I = \frac{1}{\tau_F} \int_{V_F}^{V_T} C(V)\, dV \tag{1}$$

where

$C(V)$ = diode cell capacitance,
V_T = the voltage across the diode cell at the start of a frame,
V_F = the voltage across the diode cell at the completion of a frame.

The upper integration limit will be less than V_T if the tube has capacitive lag. Maximum signal occurs when $V_F = 0$, which corresponds

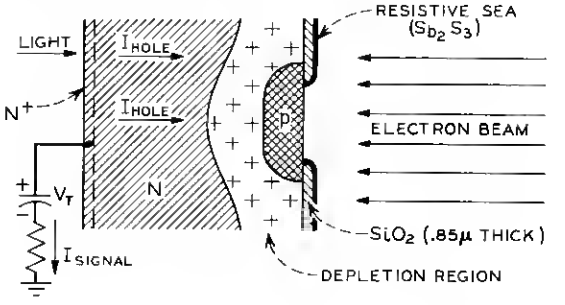

Fig. 2—Target in scanning mode.

to ideal electron beam acceptance. Additional charge storage can be obtained by driving the diode cell into forward bias. Since increased lateral hole spreading causes loss of resolution under this condition, we restrict our analysis to reverse bias conditions.

Figure 3 schematically shows the equivalent components associated with the unit cell structure. These consist of:

(*i*) tbe the diode junction capacitance, C_J ,
(*ii*) tbe the oxide capacitance, C_{ox} , and
(*iii*) the silicon surface capacitance at the silicon-oxide interface, C_{DEP} .

2.1 *Mathematical Model of a Reversed Biased Diode Unit Cell*

For purposes of analysis, an individual diode can be considered as an axisymmetric structure composed of several mathematically distinct regions. Figure 4 is a schematic representation of the analytical model. Tbe regions of interest include:

(*i*) Oxide mask— The oxide region is considered to be a homogeneous, cbarge free region witb dielectric constant ϵ_1 . Tbe potential function in this region is determined by solution of Laplace's equation.

(*ii*) P^+ diffused island—This region is considered to be at a uniform potential.

(*iii*) N-type bulk region—That portion of the N-type bulk region,

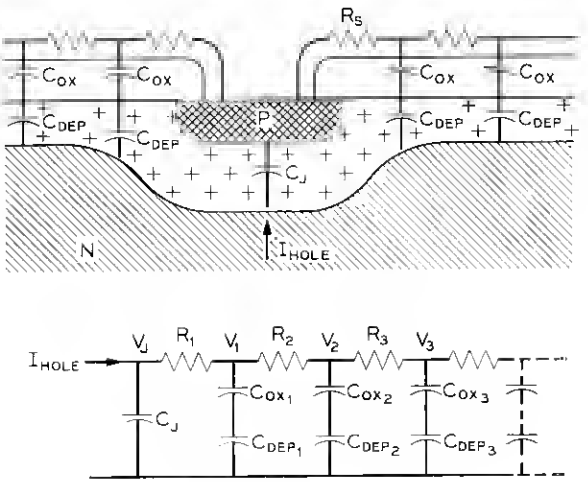

Fig. 3—Target discharge model.

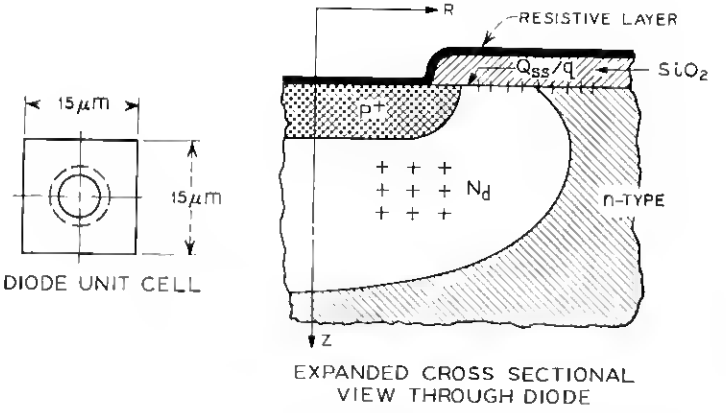

Fig. 4—Diode unit cell geometry.

remote from the depletion region, is considered to be at uniform potential.

(*iv*) Depletion region—The potential distribution in the depletion region is described by Poisson's equation. The charge distribution in the depletion region remote from the oxide-silicon interface is considered constant and set by the doping level of the N-type bulk material. An additional charge density is assumed in the depletion region at the Si–SiO_2 interface to describe the oxide fixed charge. The depletion region has a dielectric constant ϵ_2 .

2.2 *Boundary, Interface Conditions*

The target analysis is complicated because the target consists of axisymmetric diffused regions arranged on a square format and spaced such that the diode depletion regions can connect for some combinations of target parameters. We analyze an axisymmetric structure and correct for the effects of the cell corner regions when necessary.

Except for the boundary separating the depletion and N-type bulk regions (discussed in Section 2.3), the boundary conditions for this problem are straight-forward:

(*i*) There is a radial potential distribution on target surface.

(*ii*) The radial potential gradients along the axis of symmetry are zero.

(*iii*) The condition of conservation of charge flux is applied at the oxide-depletion region interface.

(*iv*) Radial potential gradients at the diode periphery are zero.

2.3 *Method of Solution*

Regions of dissimilar material constants and geometrically complicated boundaries make solution by "closed form" techniques difficult. For this reason and because of its inherent geometric flexibility, a numerical or finite difference solution was adopted.

The entire diode structure is considered to be composed of differential elements spaced on a square mesh (Fig. 5). The potential of each element is described by an appropriate difference equation which takes into account the material constants of the element and its interaction with adjacent elements. For example, the potential of an element in the depletion region at a location (I, J) is given by a difference equation of the type:

$$\epsilon A_z\left[\frac{V(I, J+1) - V(I, J)}{\Delta Z} + \frac{V(I, J-1) - V(I, J)}{\Delta Z}\right] + \epsilon A_-\left[\frac{V(I-1, J) - V(I, J)}{\Delta R}\right] + \epsilon A_+\left[\frac{V(I+1, J) - V(I, J)}{\Delta R}\right] = -q\,\Delta Z A_z N(I, J) \tag{2}$$

where

$V(I, J)$ = potential of point (I, J),
A_z, A_+, A_- = areas of element faces,
ϵ = dielectric constant,
ΔR = radial element spacing,
ΔZ = axial element spacing,
$qN(I, J)$ = charge density.

Similar difference equations can be written to describe the behavior of other regions.

Thus the potential of any element can be described by a linear algebraic equation. If the geometry of interest is described by decomposing the structure into an M by N array of such elements, then the problem is reduced to the solution of an $M \times N$ set of linear equations. For a typical geometry considered in this study, the structure was represented by a 70 by 85 array of elements. This set of equations was solved by accelerated Gauss–Seidel iteration.[5]

An important aspect of the solution of this problem is the specification of the depletion region boundary. The P^+-depletion layer boundary is defined by the doping profile. We assume a P^+ step junction. The depletion region-N-type bulk boundary is a function of impurity distribution, oxide-silicon interface charge density, and resistive sea surface

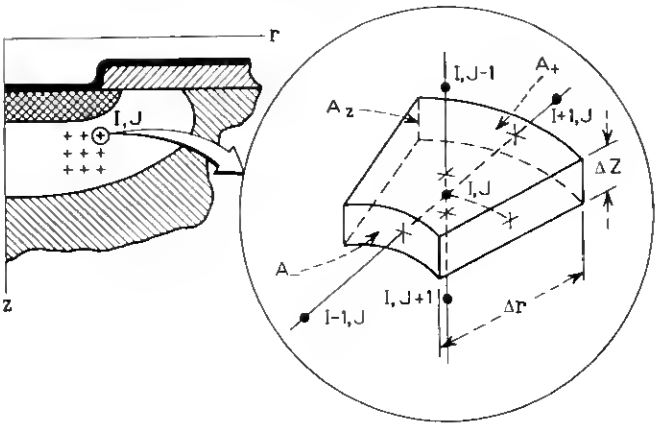

Fig. 5—Difference elements.

potential and must therefore be computed for each new combination of diode parameters. An iterative procedure was used to calculate potential and to define the limits of the depletion region. Beginning at the edge of the P^+ diffused island an iterative sweep through the potential field was made. At those points where the computed potential was less than the applied potential plus the built-in potential of the junction, V_B, Poisson's equation in difference form was applied. When a potential equal to or greater than $V_T + V_B$ was computed, the potential at that point was set equal to $V_T + V_B$. This procedure was repeated until a satisfactory solution was obtained.

2.4 *Capacitance Calculation*

Depletion region capacitance was calculated by treating the depletion boundaries as the surfaces of a two-plate capacitor. The potential field between the plates of such a capacitor was calculated by solving Laplace's equation, taking into account the different dielectric constants for the oxide and silicon regions. Charge density on the surface is given by

$$Q = \epsilon E_n , \tag{3}$$

where E_n is the normal electric field component calculated using difference approximations for the first derivative of the potential, and ϵ is the appropriate dielectric constant.

Total diode capacitance is then equal to the integral of the local charge density divided by the local voltage over the total cell surface area.

III. MATHEMATICAL MODEL OF IDEAL CELL DISCHARGE

The model considered in the analysis of signal capability is shown schematically in Fig. 3. For all subsequent calculations the target is biased at a 12-volt potential relative to the cathode (except as noted). Both cathode potential drop and beam limitations (including the effect of the resistive sea impedance in series with the P^+ island) are neglected in this portion of the analysis. These assumptions imply sufficient beam current to completely restore the target surface to cathode potential after each beam scan, re-establishing the initial 12-volt reverse bias across the junction. (With our convention reverse bias and surface potential sum to 12 volts.) During the time interval during which a diode is disconnected from the electron beam, τ_F, an array diode is discharged by the light generated hole current collected by its depletion region. As the unit cell is discharged, the P^+ island potential increases approaching 12 volts for high illumination levels. The voltage profile on the target surface depends on substrate resistivity, SiO_2–Si interface fixed charge density, target geometry, illumination level, resistive sea sheet resistance and electron beam acceptance characteristic. For the case of a very high resistance sea—that is, no lateral charge flow onto the sea—the potential of the resistive sea surface remote from the diode windows will remain at ground potential and the light generated current will act to discharge the P^+N junction only. Conversely, for the case of a low sheet resistance sea the entire resistive sea surface potential will rise nearly uniformly.

3.1 *Qualitative Description of Model*

The time dependent solution of the diode cell discharge transient is a complicated non-linear problem. However, a reasonable model for this problem should include the voltage dependence of both the junction and SiO_2–Si surface capacitances. The silicon surface capacitance is important since it acts in series with the oxide capacitance to affect the time constant of the resistive sea. For example, in the depleted mode the equivalent oxide surface capacitance can be half the oxide capacitance.

The lateral voltage drop on the diode unit cell surface makes possible the formation of an inversion layer at the SiO_2–Si interface. Since this effect can (for some combination of target parameters) establish the upper limit on sea resistance, the model should include inversion phenomenon. Strong inversion was assumed when the magnitude of the surface potential relative to the bulk semiconductor potential exceeds the junction reverse bias, V_R, by twice the magnitude of the bulk Fermi potential, ϕ_F.[6]

A quasi steady-state solution was used in which the discharge time interval was divided into sub-intervals over which the surface capacitance was assumed time invariant. The dependence of the junction capacitance on voltage was explicitly described.

An outline of the unit diode cell discharge analysis is shown in Fig. 6. For computational purposes, τ_F was divided into several equal segments. The computational sequence used during each time segment was as follows:

(*i*) At the beginning of each segment: First, the unit cell depletion geometry and corresponding surface capacitance were calculated subject to boundary conditions which include the resistive sea surface potential distribution from the previous time step. Second, the surface potential profile was recalculated to adjust for altered surface capacitance by imposing temporal continuity of surface charge.

(*ii*) Having obtained the surface potential and capacitance profiles, a transient solution to the array discharge process for the time segment

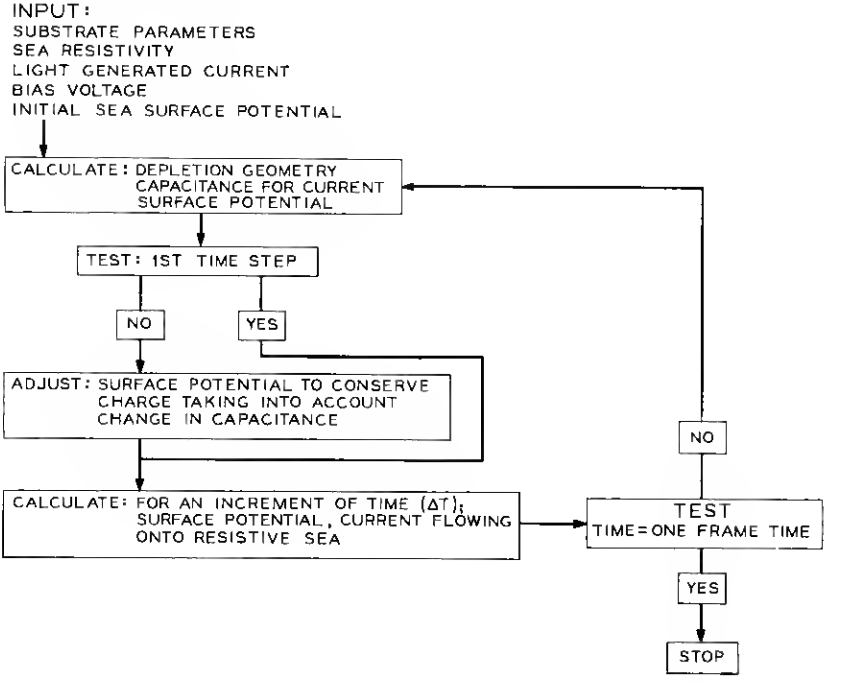

Fig. 6—Unit cell discharge analyses.

was performed with the surface capacitance profile held constant. The voltage dependence of the junction capacitance was accounted for. The time dependent surface potential profile and sea current were then calculated. The final potential profile was used in the first part of step i of the next time interval.

3.2 *Some Particular Details of Target Operation*

Target operation can be most easily characterized by considering operation either below or above total depletion of the silicon surface at the Si–SiO_2 interface. When operating below total surface depletion, variations in sea sheet resistance can alter only the width of the depletion layer at the surface. Above the condition of total surface depletion, the resistive sea sheet resistance can control the formation of a silicon surface inversion layer. It should be noted that because of geometrical effects, total surface depletion may occur in the diode array at voltages significantly below the depletion voltage which would be obtained on a MOS capacitor with the same oxide thickness and interface properties.

3.2.1 *Target Operation Below Total Surface Depletion*

Consider a 10 Ωcm substrate target with an interface fixed charge density (Q_{ss}/q) of $6 \times 10^{11}/cm^2$ and $V_T = 12$ volts. Under these conditions the target will be below total surface depletion. Figures 7 and 8 illustrate the behavior of the depletion region and resistive sea surface potential at various intervals during discharge for two values of sea resistance.

Comparison of the depletion layer geometries at $t = \tau_F$ (corresponding to full discharge) shows that the signal obtained from the junction-only capacitance is not appreciably altered by differences in sea sheet resistance. The surface potential profiles at $t = \tau_F$ clearly indicate the difference in surface charge flow for the two values of sheet resistance. An effective frame time of 1/60 second is assumed.*

Figures 9 and 10 show the corresponding sea current and junction potential variations over one frame time for the same two sea resistance values. In both cases the junction voltage reaches the 12 volt bias potential prior to the completion of the frame time. Therefore, the light discharge current specified in the calculations 6.4 pA was in excess of true saturation, and lateral hole diffusion in the bulk occurs during the latter portion of the discharge cycle. For example, for the 10^{14} Ω/□ resistive sea (Figs. 8 and 10), 3.1 pA of the 6.4 pA light signal corre-

* The system frame time is 1/30 second; however, due to the interlace scan system and large beam diameter, the diodes are charged at a 1/60 second rate.

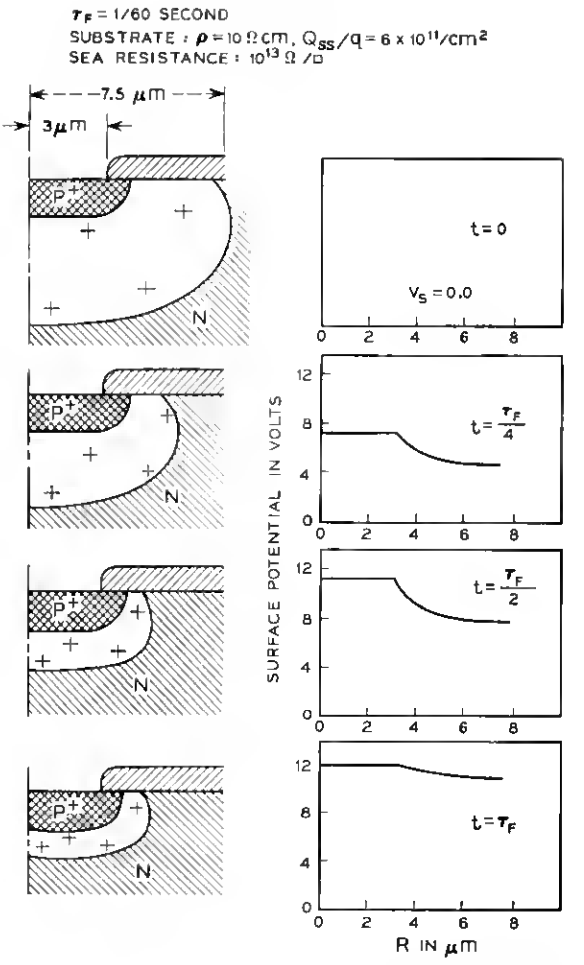

Fig. 7—Calculated discharge conditions for low sea-sheet resistance.

sponds to the discharge of the junction-only capacitance. The time-averaged sea current is 1 pA. The lateral loss due to diffusion is 2.3 pA. By decreasing the sea resistance to 10^{13} Ω/□ (Figs. 7 and 9) the average sea current is increased to about 2 pA-giving a total average cell discharge current of 5.1 pA.

3.2.2 *Target Operation Above Total Surface Depletion*

For target operation at bias voltages where the surface can be totally

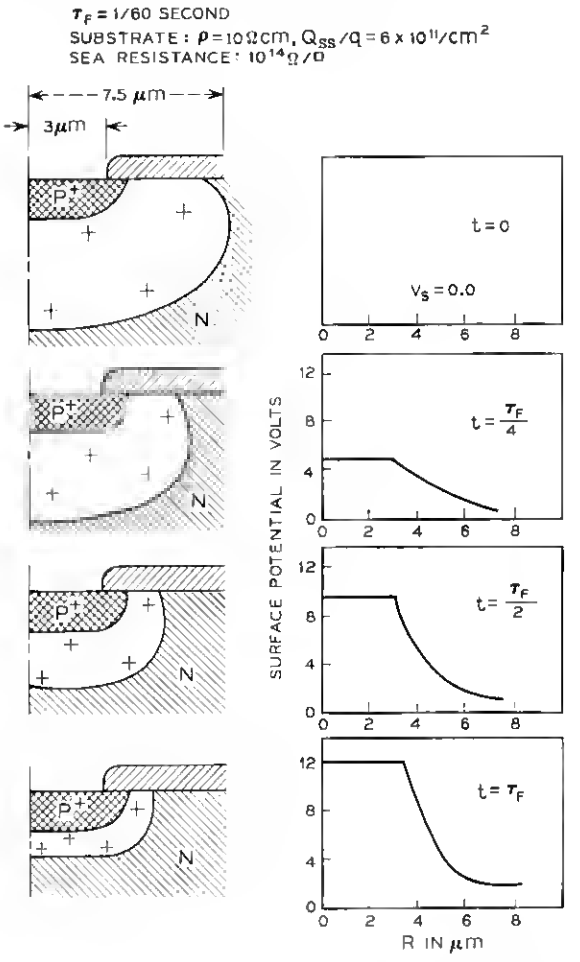

Fig. 8—Calculated discharge conditions for high sea-sheet resistance.

depleted, the sea sheet resistance is more critical. Sea sheet resistance not only controls tbe coupling of the oxide and junction capacities but can allow the formation of an inversion layer prior to total cell discharge. This effect can result in an additional limitation on maximum useful signal current. For example, consider the final depeltion region configuration (Fig. 11) for a substrate resistivity (ρ) equal to 10 Ωcm, Si–SiO_2 interface fixed charge density (Q_{ss}/q) equal to $3 \times 10^{11}/cm^2$, and a sea sheet resistance (R_s) equal to 10^{14} Ω/□. Because of the lower

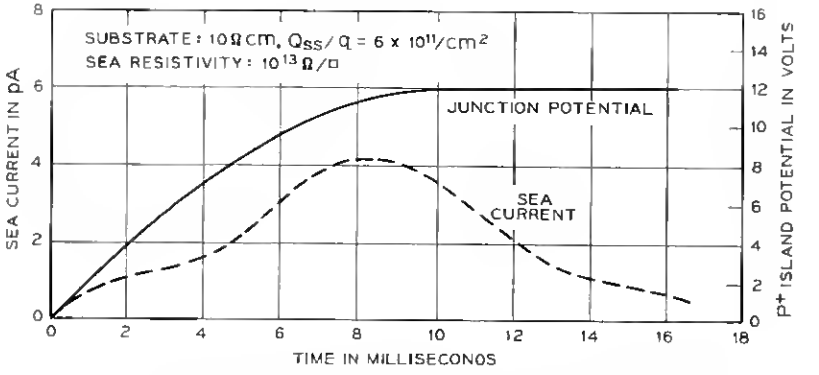

Fig. 9—Calculated discharge characteristics for low sea-sheet resistance.

Q_{ss}/q, the depletion region is markedly different from that of the unit cell previously considered (Figs. 7 and 8). Note that the depletion layer exists even at the end of the frame time. Furthermore, the final discharged condition shows surface inversion under part of the oxide surface. If the inversion layer acts to interconnect adjacent P^+ islands, then loss of resolution will occur.[4] Resolution loss does not occur simply by the existence of an inversion layer but rather when sufficient current flow occurs between the P^+ island and the inversion layer to connect adjacent P^+ islands. To investigate the formation of the inversion layer, it is necessary to examine the $Si–SiO_2$ interface potential distribution. Figure 12 shows the potential profile (for $Q_{ss}/q = 2 \times 10^{11}/cm^2$ and $R_s = 1.5 \times 10^{14}\ \Omega/\square$) at three time intervals in the discharge cycle. It can be seen that all the light-generated minority carriers which reach

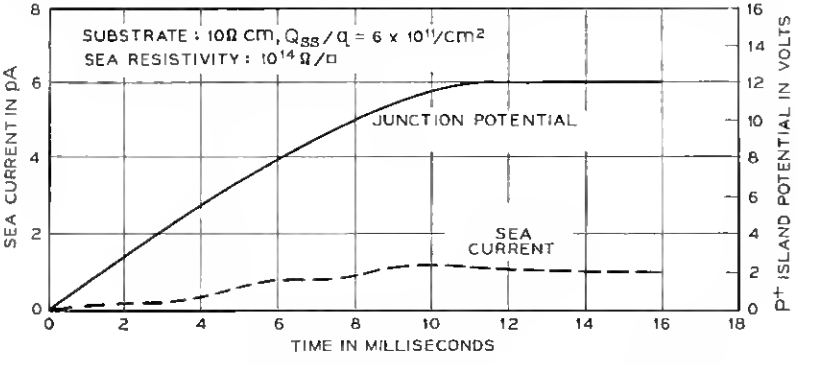

Fig. 10—Calculated discharge characteristics for high sea-sheet resistance.

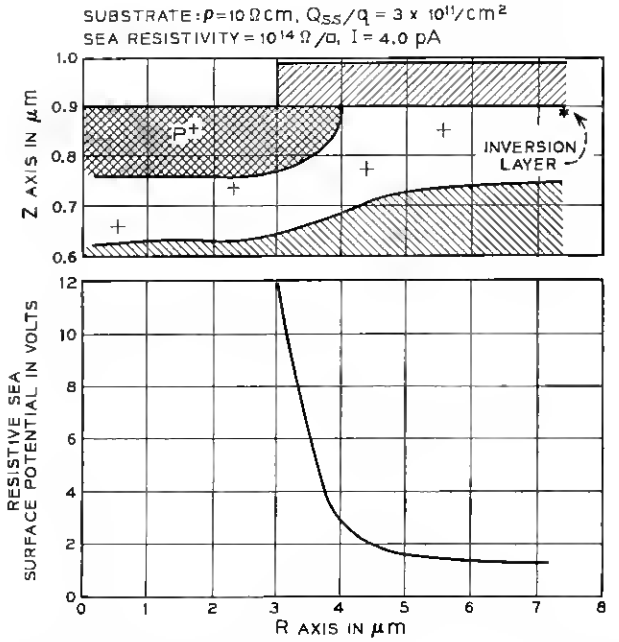

Fig. 11—Calculated discharged conditions for above total surface depletion operation.

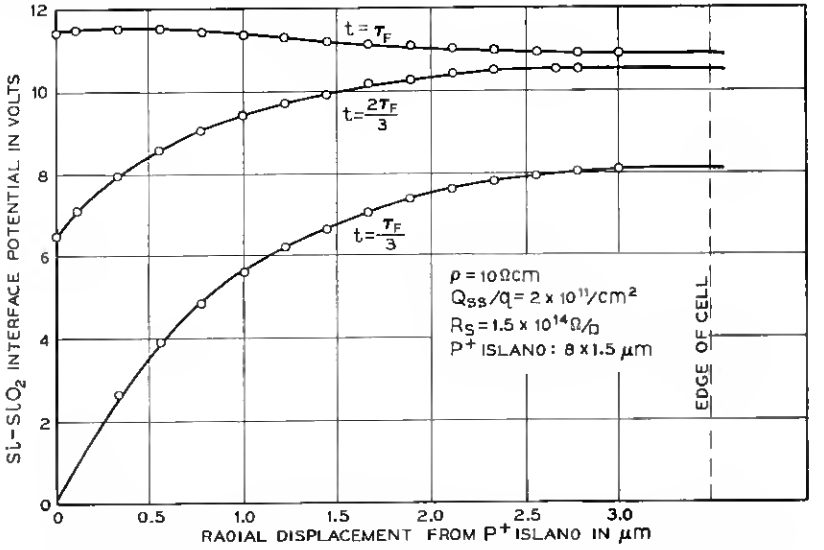

Fig. 12—Si–SiO_2 interface potential at the end of three equal time intervals during discharge.

the depletion region are collected by the P^+ island until that time, late in the discharge cycle, when the silicon surface potential remote from the P^+ island drops to below the P^+ island potential. This condition only occurs for high sea-sheet resistance which causes a large radial voltage gradient on the sea surface.

Figure 13 illustrates the Si–SiO_2 interface potential distribution relative to the P^+ island potential at the end of the discharge cycle for several values of light-generated current. This figure shows that for low current levels a potential barrier for holes exists between the P^+ island and inversion region. The magnitude of this barrier decreases as the junction current is increased. We have assumed that loss of resolution occurs when this potential barrier drops below $2kT$. For this particular example, the diodes effectively interconnect at a light-generated current of 2.1 pA, and the strongly inverted layer need only extend to within 2.6 μm of the P^+ island.

IV. TARGET SIGNAL CAPABILITIES

In this section calculated results are presented which illustrate the general effect of diode parameters and operating bias on target signal capabilities.

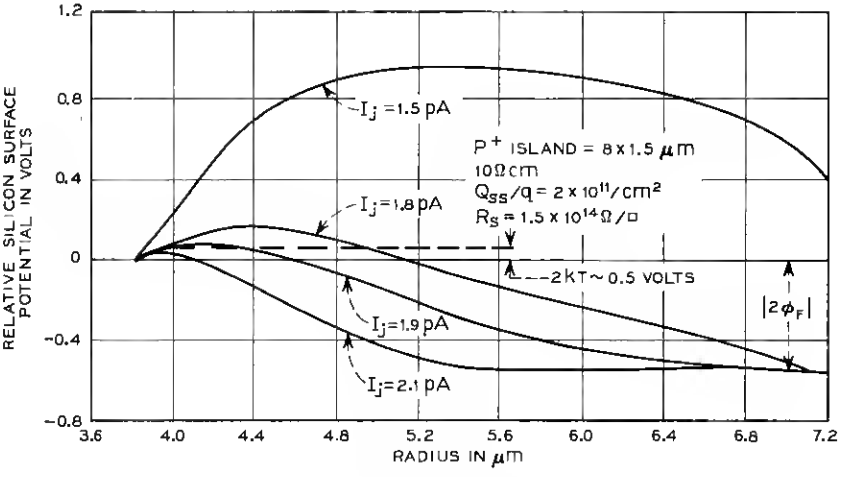

Fig. 13—Si–SiO_2 interface potential relative to P^+ island potential at completion of the discharge cycle for several levels of light-generated discharge current.

4.1 *Effect of Signal-Limiting Mechanisms*

Signal current characteristics of target arrays fabricated on 10 Ωcm substrates with Q_{ss}/q equal to 1, 2, and 3 × 10^{11}/cm^2 are shown in Fig. 14. This figure graphically illustrates the interdependence of the SiO_2–Si

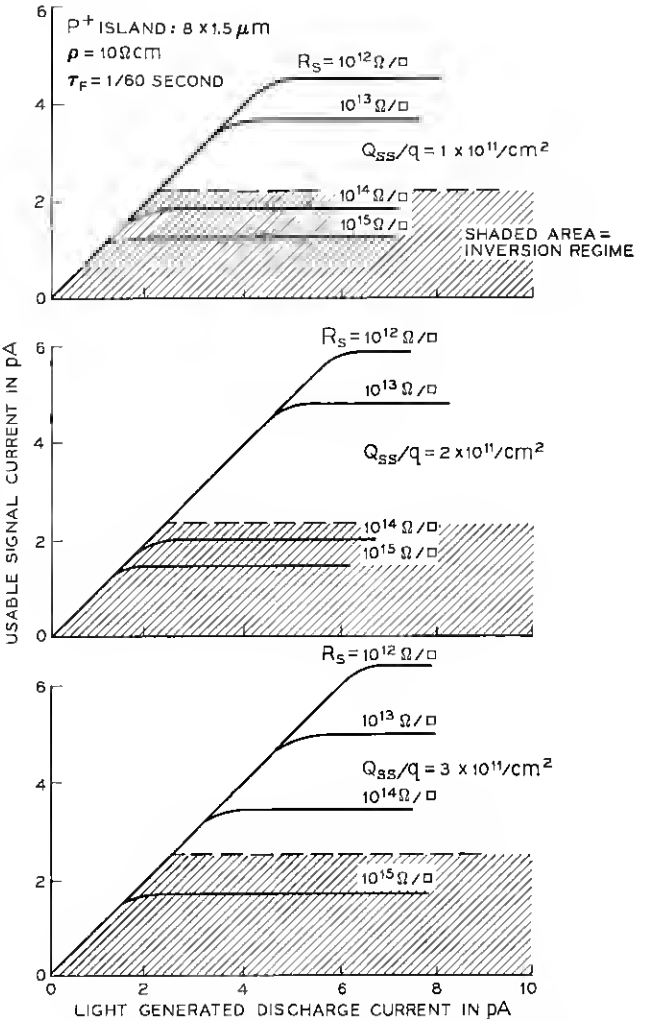

Fig. 14—Effect of Q_{ss}/q on single cell signal current characteristics.

interface charge density and sea sheet resistance on signal current characteristics.

Oxide-silicon interface fixed charge density affects the array signal capacity for all values of sea resistance. For example, consider a target fabricated with a low sea sheet resistance of 10^{12} Ω/□. If this array bas an interface fixed charge density of $3 \times 10^{11}/cm^2$, it will provide a 6.4 pA signal current per diode. A similar target having a fixed density of $1 \times 10^{11}/cm^2$ is capable of only 4.5 pA per diode. Using an estimated minimum sea resistance consistent with resolution,[4] of $R_S = 10^{13}$ Ω/□, the maximum usable signal current per diode is 5 pA for $Q_{ss}/q = 3 \times 10^{11}/cm^2$; and 3.6 pA for $Q_{ss}/q = 1 \times 10^{11}/cm^2$.

For high sea-sheet resistances, above 10^{13} Ω/□, the effect of fixed interface cbarge density on signal is even more pronounced since the inversion mechanism becomes operative. Consider the case of $R_S = 10^{14}$ Ω/□. From Fig. 14 we see tbat for $Q_{ss}/q = 3 \times 10^{11}/cm^2$, the available signal is 3.4 pA/diode. If, however, the interface fixed charge is reduced to $1 \times 10^{11}/cm^2$, the inversion mechanism becomes operative and the maximum usable signal current is reduced to 1.8 pA.

4.2 *Specific Examples of Geometric Effects*

Certain combinations of P^+ island geometry, interface fixed cbarge, and sea resistance can result in a limitation in the dynamic signal capability of the target due to diode interconnection caused by silicon

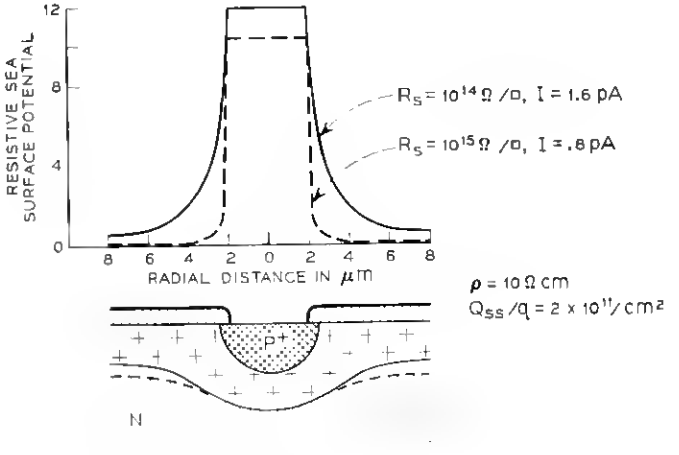

Fig. 15—Discharged conditions for 4 μm window diode.

surface inversion. Consider the three geometries shown in Figs. 15, 16 and 17 which illustrate the effect of two values of sea resistance on maximum signal current. The resistive sea potential immediately after the electron beam scan is assumed to be zero volts. The final surface potential and depletion region geometry are shown for the maximum discharged condition.

In this example, the maximum P^+ island surface potential is limited to 10 volts for the 4 μm window geometry and $R_s = 10^{15}\ \Omega/\square$; this corresponds to a signal current of 0.8 pA. Signal current for this same geometry with $R_s = 10^{14}\ \Omega/\square$ is 1.6 pA. The difference in signal currents results from surface inversion at the higher value of sea resistance. This current-limiting effect is less pronounced for the larger diode diameters as illustrated in Figs. 16 and 17. The effect of P^+ island diameter on signal current characteristics for $Q_{ss}/q = 1$, 2 and 3 $\times$ $10^{11}/cm^2$ is shown in Figs. 18 through 20. These figures graphically illustrate the interdependence of the SiO_2–Si interface charge density and sea sheet resistance on signal current characteristics.

The junction depth for the diode configurations of Figs. 18, 19, and 20 is 2.5 μm. Junction depth has a pronounced effect on signal current capabilities for values of sea sheet resistance greater than $10^{14}\ \Omega/\square$ as shown in Fig. 21. In this example, a 1.5 μm deep junction will experience

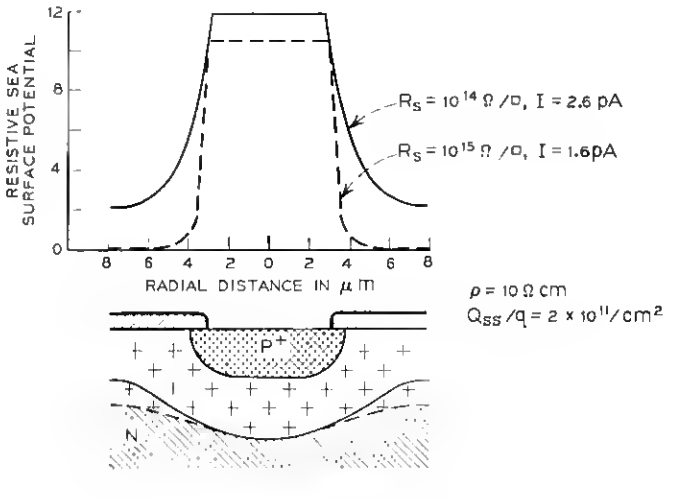

Fig. 16—Discharged conditions for 6 μm window diode.

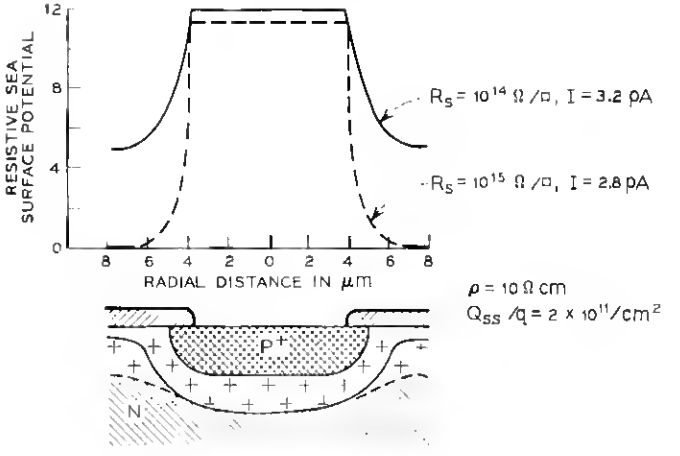

Fig. 17—Discharged conditions for 8 μm window diode.

a 43 percent signal limitation due to surface inversion compared with a 2.5 μm deep junction of the same diameter.

The effect of target bias on usable signal current has also been investigated. Increased target bias reduces usable signal for targets with high sea resistance and low interface fixed-charge density. Signal capabilities of targets operated at 12- and 16-volt bias can be compared

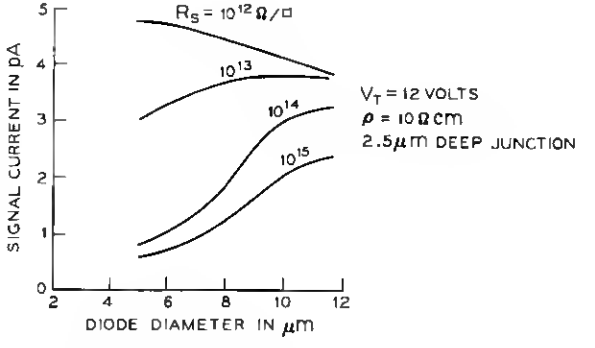

Fig. 18—Single diode signal capability for $Q_{ss}/q = 1 \times 10^{11}$ cm^{-2}.

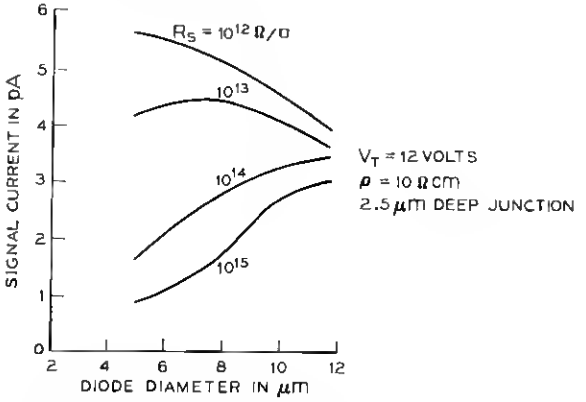

Fig. 19—Single diode signal capability for $Q_{ss}/q = 2 \times 10^{11}$ cm^{-2}.

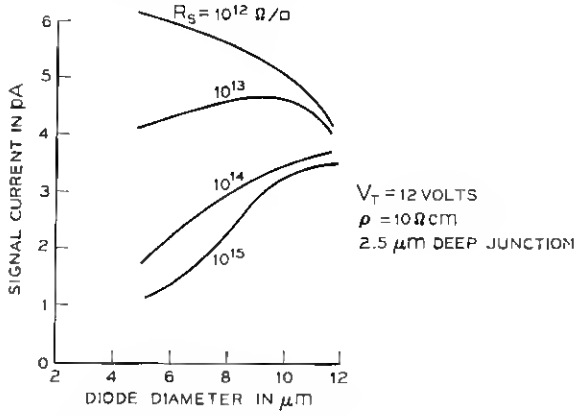

Fig. 20—Single diode signal capability for $Q_{ss}/q = 3 \times 10^{11}$ cm^{-2}.

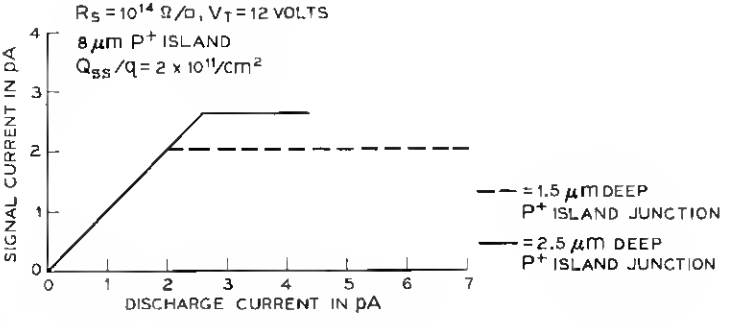

Fig. 21—Effect of P^+ island depth on single diode signal characteristic.

in Fig. 22. For R_s greater than 10^{14} $\Omega/\square$, reduction of usable signal for the higher bias case is due to inversion effects caused by larger sea surface-potential gradients.

V. EFFECT OF ELECTRON BEAM ACCEPTANCE

In order to estimate the effects of electron beam acceptance on signal characteristics, the following experimental-analytic approach was undertaken:

(*i*) A mathematical model of the charge-discharge mechanism of the target in the scanning mode was established.

(*ii*) For several target bias conditions, maximum signal current (maximum light level consistent with resolution) and the residual signal characteristic were measured. The residual signal lag was measured by chopping the target illumination as described in Section 5.2.

(*iii*) Fabrication parameters for this target (Q_{ss}/q, P^+ island geometry, sea resistance and substrate resistivity) were measured.

(*iv*) The junction-only capacitance-voltage characteristic was calculated from measured target parameters. In this instance, sea resistance was sufficiently high so that the junction-only capacitance was the only signal-generation mechanism.

(*v*) Using the capacitance voltage characteristic of the junction, the saturation signal and lag characteristics of the tube, and the mathematical representation of the target charge-discharge mechanism; a beam-landing function was generated by a trial and error procedure which satisfies these measured characteristics. In this calculation the contribution to lag of interface trapping states was neglected.*

(*vi*) Using the beam landing characteristic thus generated and the mathematical model, lag and beam limited signal were calculated for various diode P^+ island geometries.

5.1 *Signal Limitations*

The resulting signal current versus P^+ island diameter for a junction depth of 2.5 μm is given in Fig. 23. Comparison of these results with those for perfect beam landing shows that the beam limitation causes a significant reduction in target signal capability. For example, a diode having 8 μm P^+ island diameter and a 10^{14} $\Omega/\square$ sea sheet resistance has a maximum signal current capability of 2.8 pA. With beam limitation, signal current is reduced to 1.0 pA. It should also be noted that the beam

* G. F. Amelio has shown that under some conditions trapping states at the oxide-silicon interface can contribute to target lag.

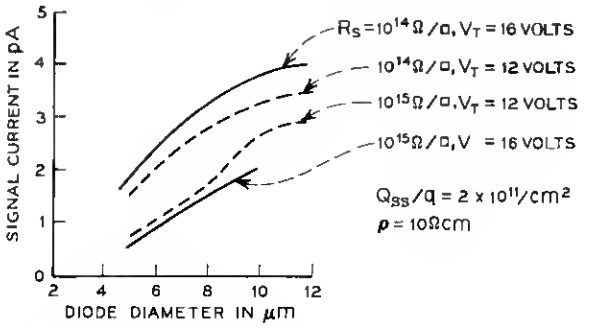

Fig. 22—Effect of bias on single diode signal capability.

current limitation will accentuate surface inversion for the higher values of sea resistance. As one might expect, larger diameter oxide windows improve beam collection efficiency and thus minimize signal limiting.

The effect of beam acceptance on the surface inversion phenomenon is illustrated in Fig. 24. This figure shows the locus of operation voltages as a function of light level for an 8-μm P^+ island diameter and a sea resistance sufficiently high to decouple the oxide capacitance. As light-generated discharge current level increases the maximum target surface potential approaches the target bias. For a sea resistivity of 10^{14} $\Omega/\square$ the maximum allowable P^+ island potential can rise to the 16 volt bias potential without diode interconnection due to silicon surface inversion. If beam limitation is taken into consideration, the calculated potential swing is 12 to 16 volts resulting in a maximum signal level of 1.2 pA per diode. If the sea sheet resistance is increased to 10^{15} $\Omega/\square$, surface inver-

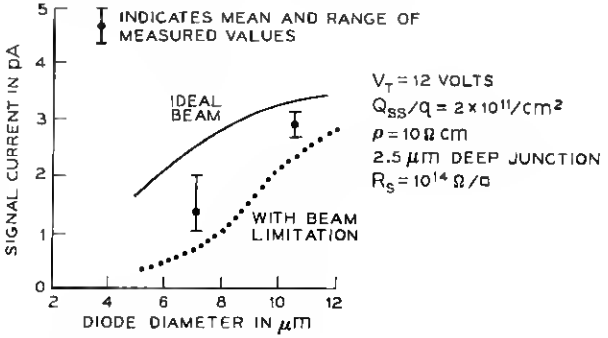

Fig. 23—Effect of electron beam acceptance on single diode signal capability.

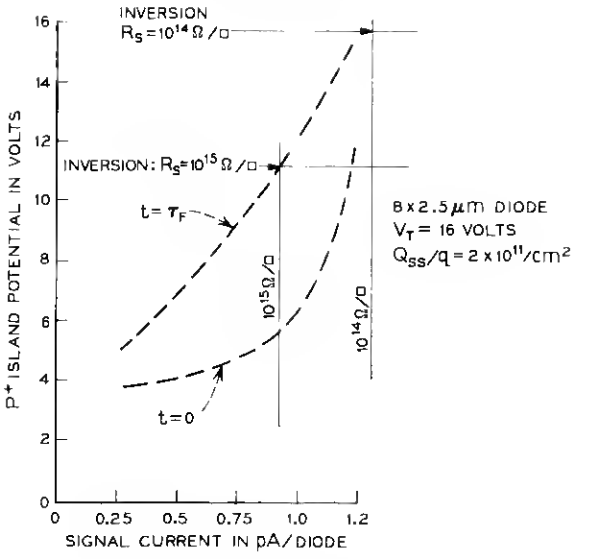

Fig. 24—Calculated P^+ island potential extremes as a function of discharge current.

sion limits the P^+ island potential to 11.0 volts. The maximum signal current for this case is therefore only 0.9 pA.

5.2 *Capacitive Lag—Transient Illumination*

Thus far only time invarient illumination of the target has been considered. Non-ideal beam landing results in capacitive lag for transient illumination conditions. The definition of lag used here is illustrated in Fig. 25. Light is left on for a sufficient time interval for the target to assume steady state operation; that is, $\Delta Q_{charge} = \Delta Q_{discharge}$. The light is then turned off and the instantaneous signal current at subsequent scanning intervals determined. Lag is then defined as the ratio of the signal current at 1/15 second after the light is turned off to the steady-state illuminated signal.

Lag is a function of the resistive sea impedance, the diode capacitance, and the electron beam acceptance. The electron beam acceptance is a function of the resistive sea surface potential. Since both the instantaneous diode capacitance and the sea surface potential are determined by the level of light-generated cell discharge current, lag is also a function of signal level as illustrated in Fig. 26. For the case under consideration, two effects are evident:

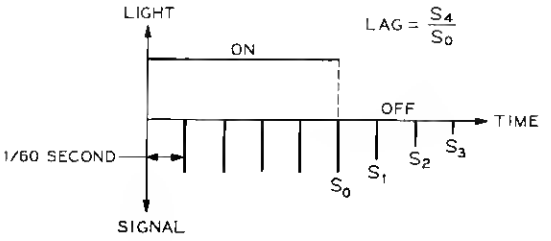

Fig. 25—Definition of lag.

(*i*) At higb signal levels lag is enhanced by large target cell capacity.
(*ii*) At low ligbt levels, where cell capacity is reduced, poor beam acceptance increases lag.

The result for this example is a minimum lag condition at less than maximum signal current. Since this effect is a strong function of the electron beam acceptance cbaracteristic, the width of the lag minimum can vary considerably from tube to tube.

VI. ALTERNATE TARGET STRUCTURE

Tbe occurrence of inversion effects can be minimized, but not eliminated, by fabricating targets with greater tban 10 μm diameter P^+ islands.

Inversion effects may also be controlled by means of a partial conductive overlay structure.

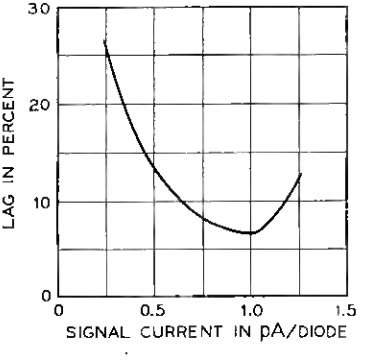

Fig. 26—Calculated lag characteristic.

6.1 *Description of Overlay Structure*

This structure is essentially that of the standard resistive sea silicon target array except conductive buttons have been formed in the oxide windows and extend over the adjacent oxide.

6.2 *Analysis*

The analysis of this structure is performed assuming that the sea region between buttons is at ground potential (a worst case condition) with a uniform potential V_T assigned to the P^+ island and conductive overlay.

Signal capabilities of this structure were also determined by calculation of the capacitance voltage characteristic of the button. Again the sea region was assumed to be at zero potential and thus electrically isolated from the junction button.

6.3 *Conductive Overlay Characteristics*

Depletion region geometries for a range of conductive overlays diameters are shown in Fig. 27. For the assumed 12 volt bias three distinct silicon surface conditions are represented by these examples:

(*i*) Separation of P^+ island from the peripheral surface inversion region by a neutral N region at the interface. This corresponds to a 11.2 μm diameter button.

(*ii*) Continuous depletion layer through the diode unit cell. For a 9.5 μm diameter button the inversion layer formed at the periphery is isolated from the P^+ island by an appreciable potential barrier.

(*iii*) Continuous depletion layer through the diode unit cell and electrical interconnection of the P^+ island and the surface inversion regions. This condition exists for the 8.0 μm diameter button.

For the 9.5 μm button, which represents the minimum diameter necessary to prevent diode interconnection for the example under consideration, the maximum signal current is 1.9 pA/diode. This is slightly less than the current obtainable with a resistive sea structure with 10^{14} $\Omega/\square$ sea sheet resistance.

The major advantage of a properly fabricated conductive overlay structure is the elimination of inversion effects (which include signal limiting and video "blooming" phenomenon) inherent in the resistive sea type targets operated with total surface depletion. While elimination of inversion effects can be accomplished by controlling sea resistance (within the range of 1 to 5 $\times$ 10^{13} $\Omega/\square$ for $Q_{ss}/q \approx 10^{11}/\text{cm}^2$) in con-

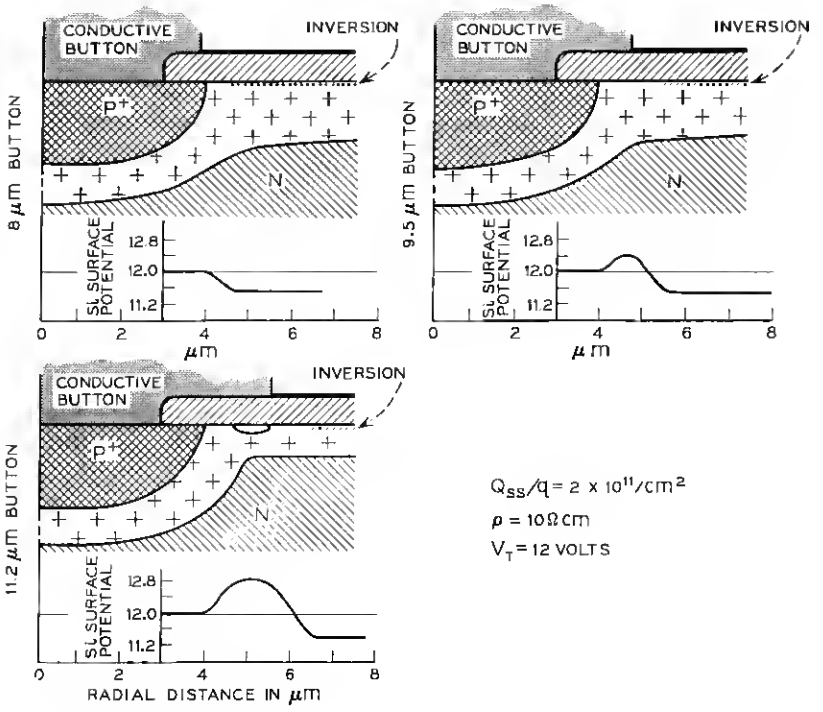

Fig. 27—Effect of conductive overlay diameter on diode discharged condition.

junction with large diameter P^+ islands (>10 μm), the button technique offers several fabrication advantages:

(*i*) Allowable range of sea resistance can be extended to 10^{13} to 10^{15} Ω/□.

(*ii*) For this structure, the critical parameters are easily measured physical dimensions, that is, diffused island and button diameters. Furthermore, the button diameter is not particularly critical provided it is larger than some minimum (approximately 1.5 μm greater than the P^+ island diameter). The maximum diameter is of course restricted to less than the diode center to center spacing, permitting substantial latitude on button size. However, two important fabricational restrictions must be observed. To assure signal uniformity the button diameter must be uniform over the diode array. Non-uniformities will be evident under light saturated signal conditions where the oxide capacitance contributes a significant portion of the signal. The second requirement

is that the P^+ island diameter be controlled to assure that the overlay will extend the required distance past the P^+ island edge to avoid inversion effects.

VII. DARK CURRENT

Surface area and volume components of the unit cell depletion region can be calculated as a function of target bias (see Fig. 28). Assuming that target dark current is the linear summation of the bulk and surface components, this geometric data, with appropriate scaling factors can be used to calculate the dark current characteristic, that is, assuming the surface component of dark current is given[7] by

$$I_s = \frac{N}{2} qn_i S_0 A_s \tag{4}$$

where

S_0 = surface recombination velocity in cm/second,
A_s = depleted silicon surface area of unit cell,
n_i = intrinsic carrier concentration,
N = number of diodes,
q = electronic charge,

and the bulk component is

$$I_{\text{bulk}} = \frac{N}{2} qn_i \frac{V}{\tau_g} \tag{5}$$

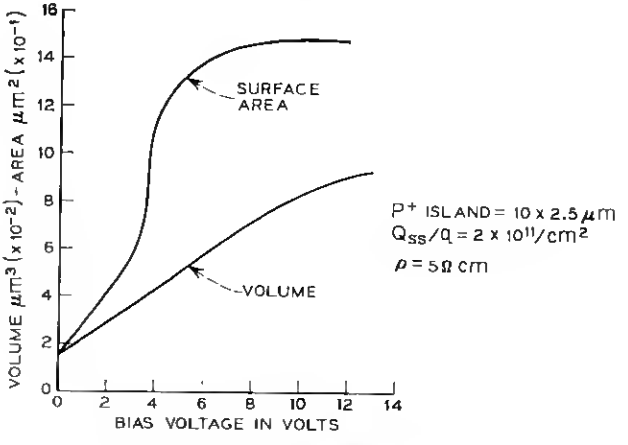

Fig. 28—Calculated depletion region geometric factors.

where

V = depleted unit cell volume,
τ_g = effective bulk generation lifetime.

For example, Fig. 29 illustrates the application of the above using measured values of S_0 and τ_g and compares this result to the measured dark current characteristic.

Figure 30 shows a family of dark current characteristics for a target with 5×10^5 diodes normalized to bulk and surface generation rates for a specific geometry. A 3-volt offset is used to account for beam limitations.

A plot of dark current versus diode diameter for 10 Ωcm material, $Q_{ss}/q = 3 \times 10^{11}/\text{cm}^2$, and $V_T = 12$ V is presented in Figure 31. It is clear, when operating above flatband, that a large P^+ island diameter improves the dark current by reducing the depleted surface area.

VIII. SUMMARY

The material presented thus far represents the results of a mathematical modeling of the silicon diode array. To be of practical use in target design the model must accurately represent target behavior. Since the complicated nature of the problem at hand precludes the normal testing of mathematical models by reduction to simplified cases, an experimental verification of the model's accuracy is the only recourse. In this section we present some comparisons of the calculated and experimentally measured target behavior. We also draw some general conclusions concerning target design.

8.1 *Comparison of Experimental and Calculated Results*

Determination of the target depletion region geometry is fundamental to the analysis of target performance. The most convenient experimental verification of the accuracy of these calculated depletion region geometries is to compare the calculated depletion region capacitance for the case of a uniform surface potential with the measured capacitance of an array covered with a metallic overlay or dot. Figure 32 illustrates such a comparison. The solid curve represents the calculated C–V characteristic for a target with a SiO_2–Si interface fixed charge density of $2 \times 10^{11}/\text{cm}^2$ and a resistivity of 5 Ωcm. The measured values were scaled from a gold dot covering 560 diodes. Notice the excellent agreement between the calculated curve and experimental measurements.

A statistical comparison of theory with measured signal current

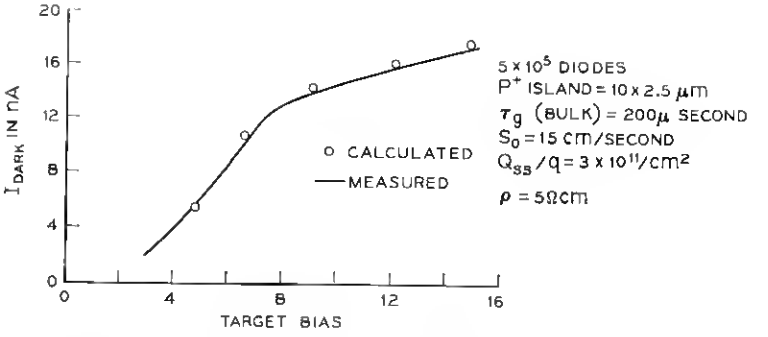

Fig. 29—Comparison of measured and calculated dark current characteristic for 5×10^5 diode array.

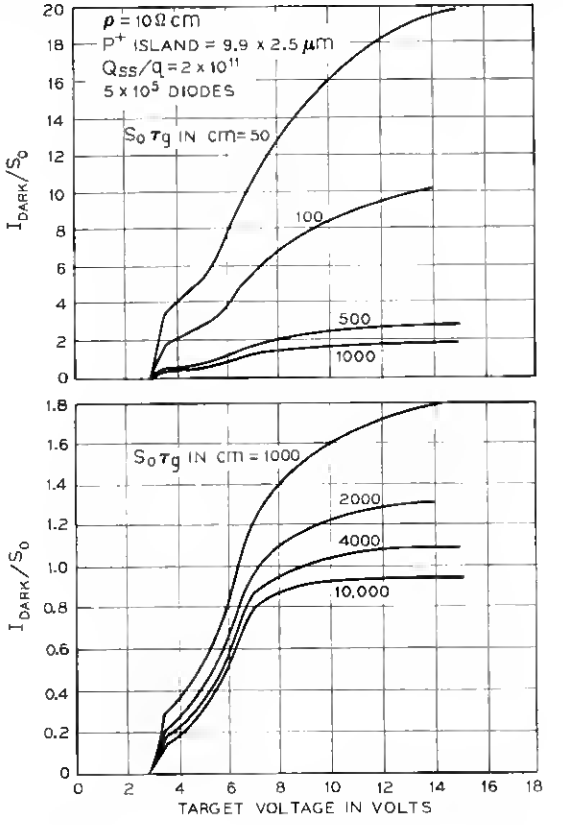

Fig. 30—Calculated normalized dark current characteristics for 5×10^5 diode array.

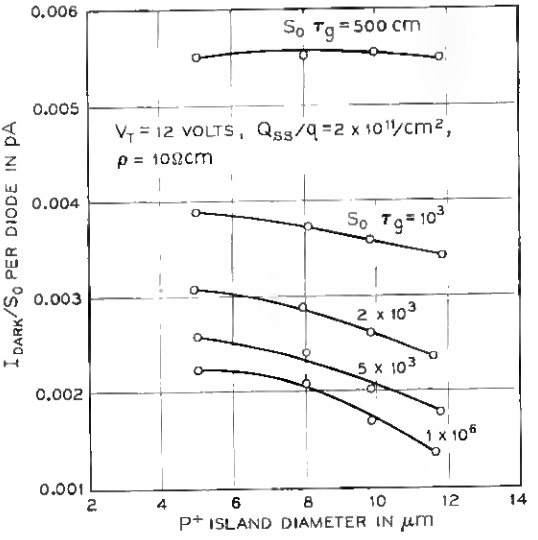

Fig. 31—Calculated relationship between dark current and P^+ island diameter.

versus diode diameter is given in Fig. 23. The range in measured maximum signal current reflects the normal variations in beam acceptance and sea resistance.

A comparison of calculated and measured dark current characteristics is illustrated in Fig. 29 for an array with measured parameters. It can be seen from these results that the bulk and surface components of dark current calculated from the depletion region geometric parameters and measured generation rates provide an adequate model for dark current.

8.2 *Some Generalizations on Target Array Geometry*

In general, several observations of the effect of target diode geometry on signal current can be made:

(*i*) For high sea sheet resistance ($\geqq 10^{14}\ \Omega/\square$) larger diameter diodes have greater signal capabilities.

First, for the case where signal is not limited by inversion this result is due to the simple geometric effect of having a larger capacitance associated with the junction.

Second, for the case where signal is limited due to surface inversion, larger diameter P^+ islands have the effect of delaying the onset of inversion (higher P^+ island potentials are possible).

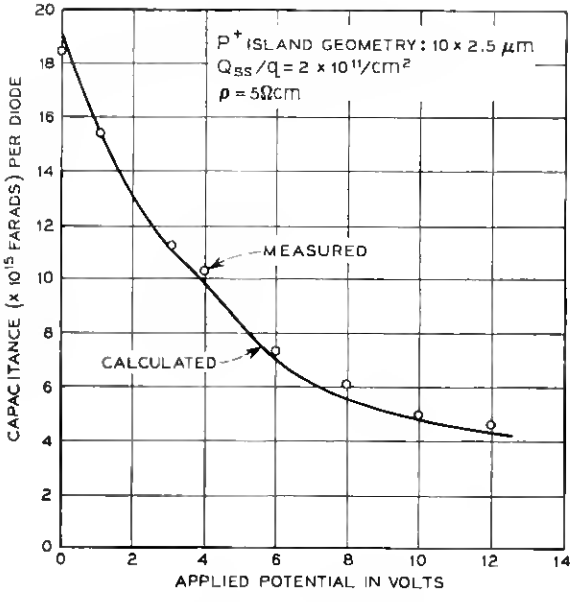

Fig. 32—Comparison of measured and calculated capacitance—voltage characteristic.

Third, increased beam acceptance for large oxide window diameter reduces both lag and signal limitations.

(*ii*) For the case where the major portion of diode leakage current is due to surface generation, increased P^+ island diameter reduces dark current due to the geometric effect of minimizing available current generating surface.

(*iii*) Silicon interface inversion effects can also be controlled by use of conductive overlay whose diameter exceeds the P^+ island diameter by 1.5 μm.

IX. ACKNOWLEDGMENTS

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